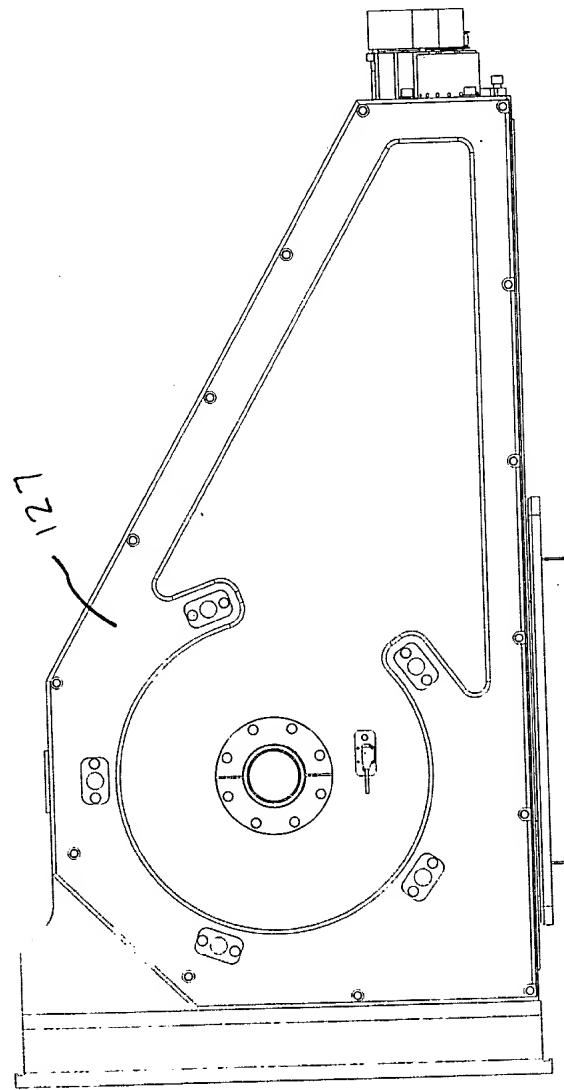


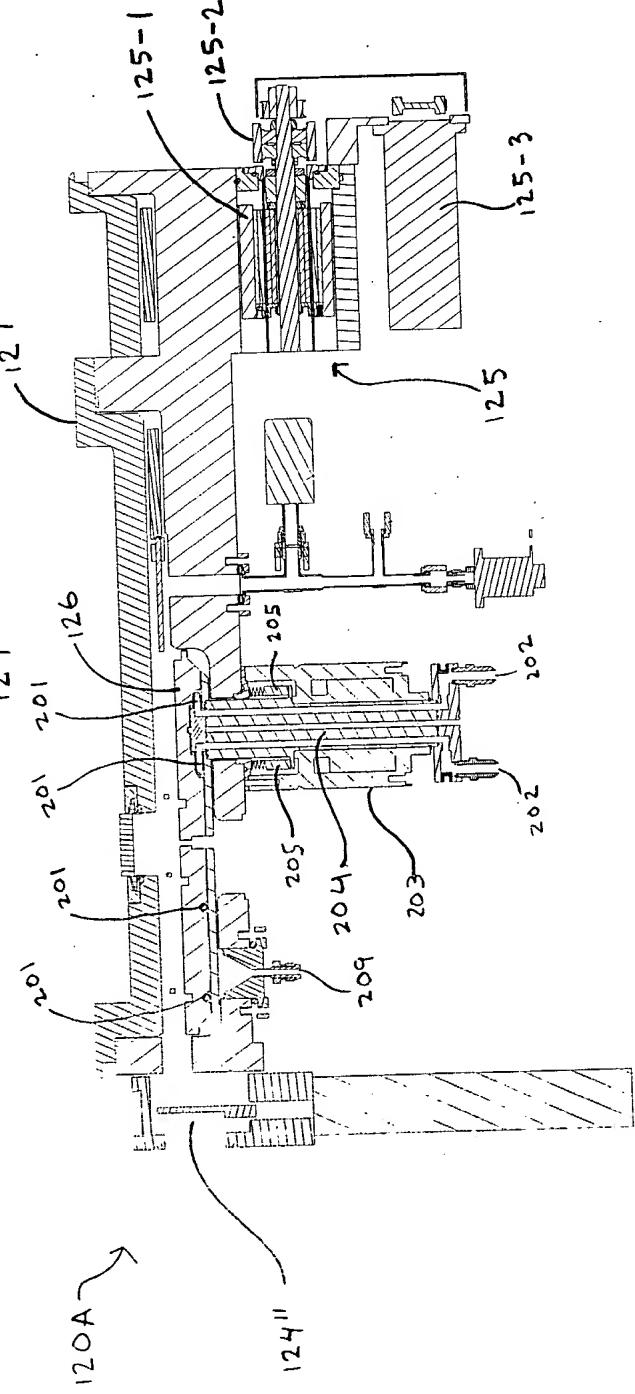
FIG. 2A

FIG. 2B



120A

FIG. 2C



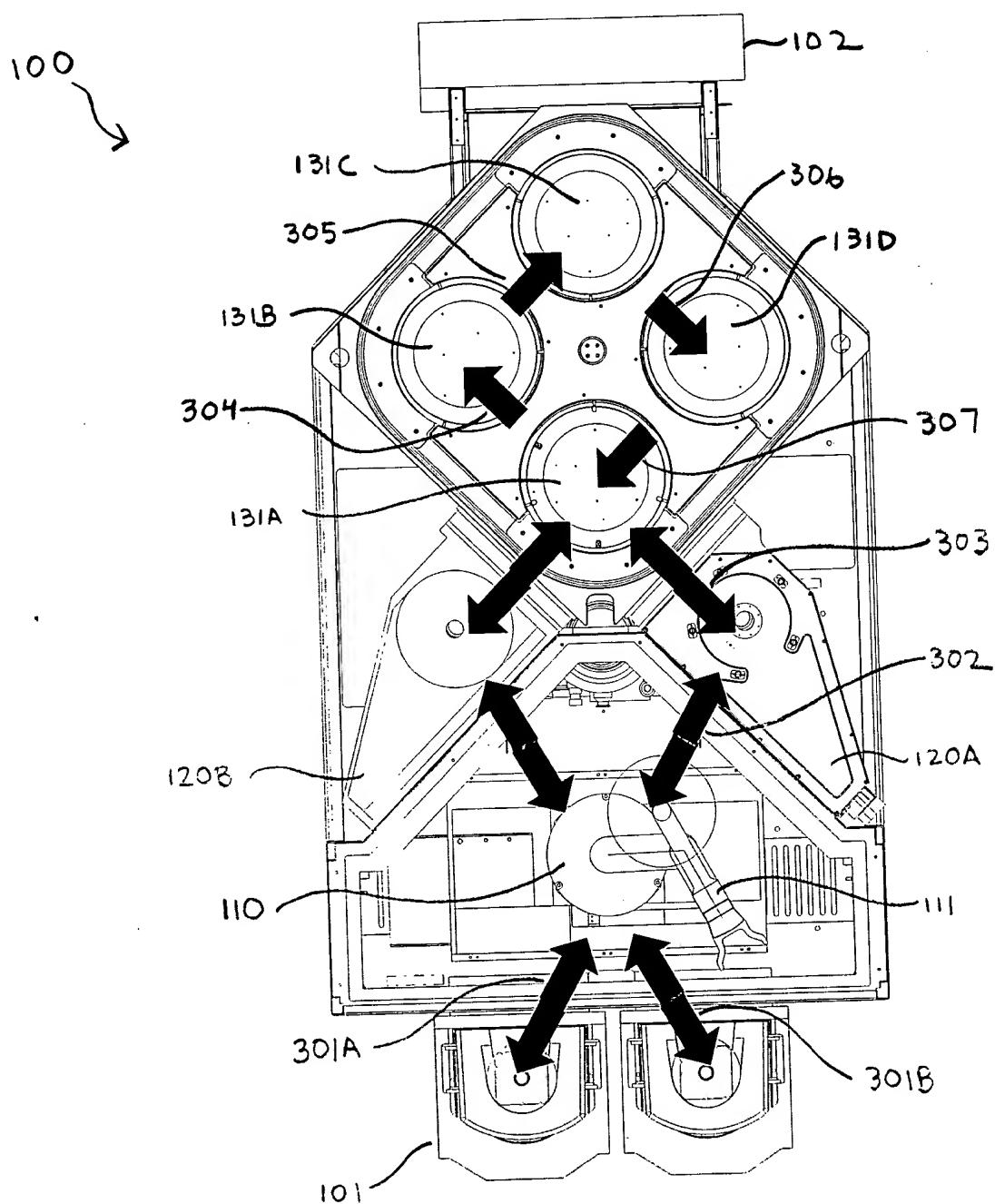


FIG. 3

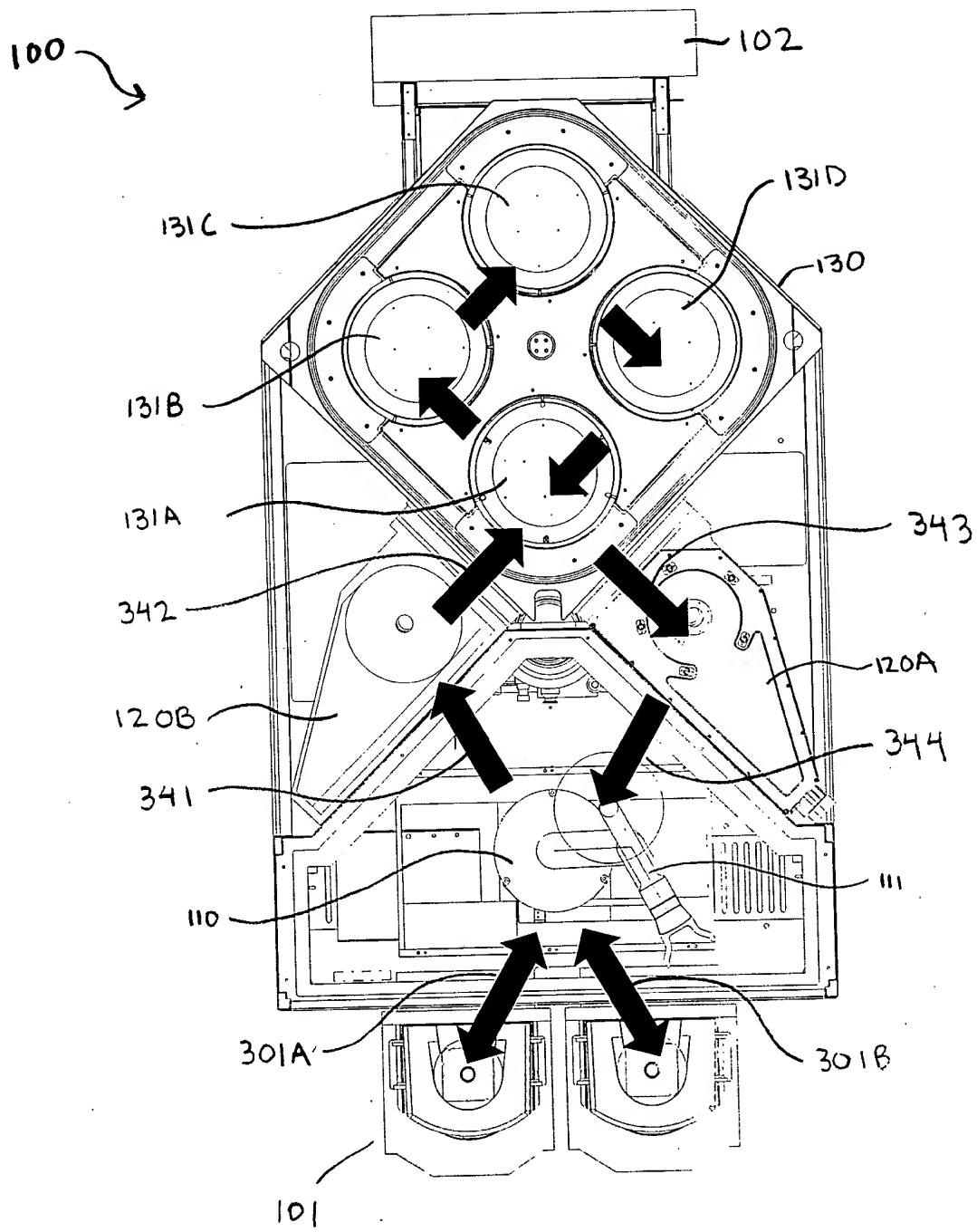
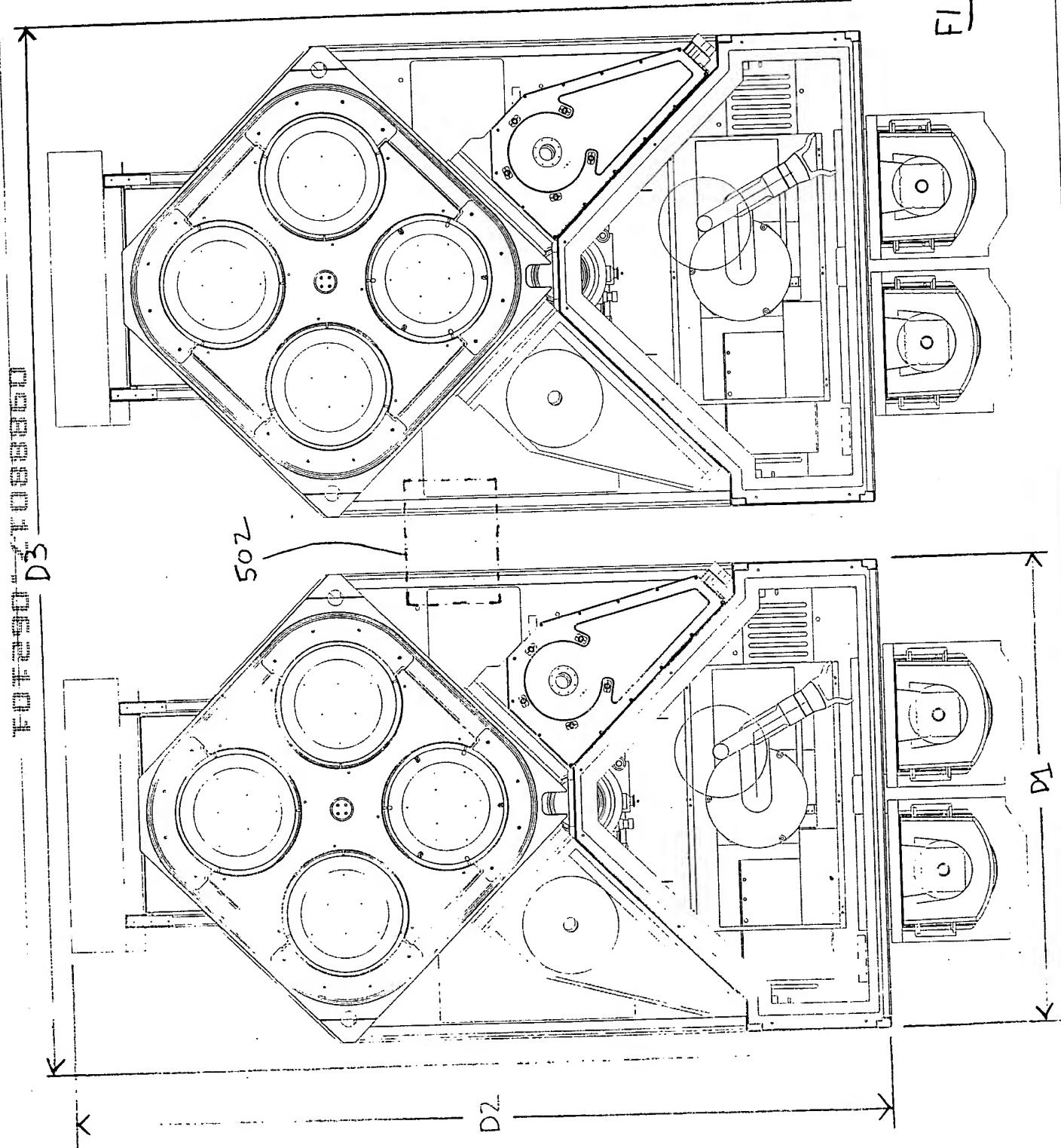


FIG. 4

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TITLE: HIGH THROUGHPUT ARCHITECTURE FOR
SEMICONDUCTOR PROCESSING

FIG. 5



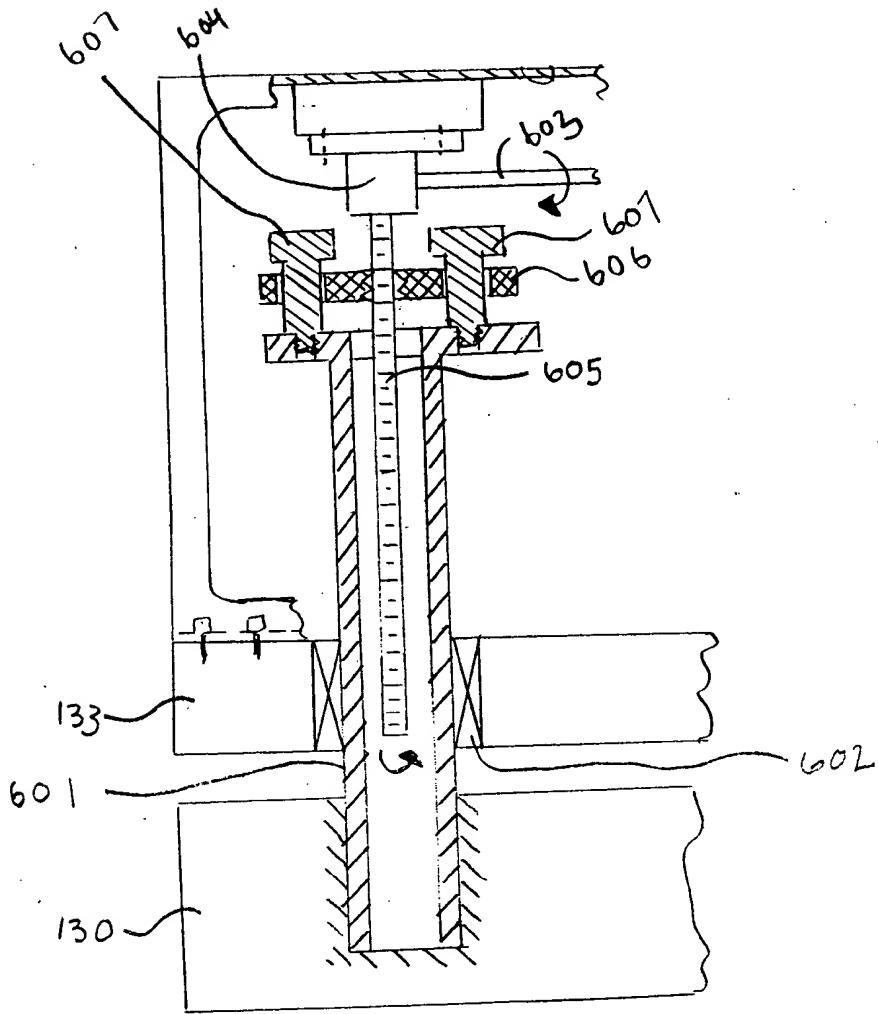
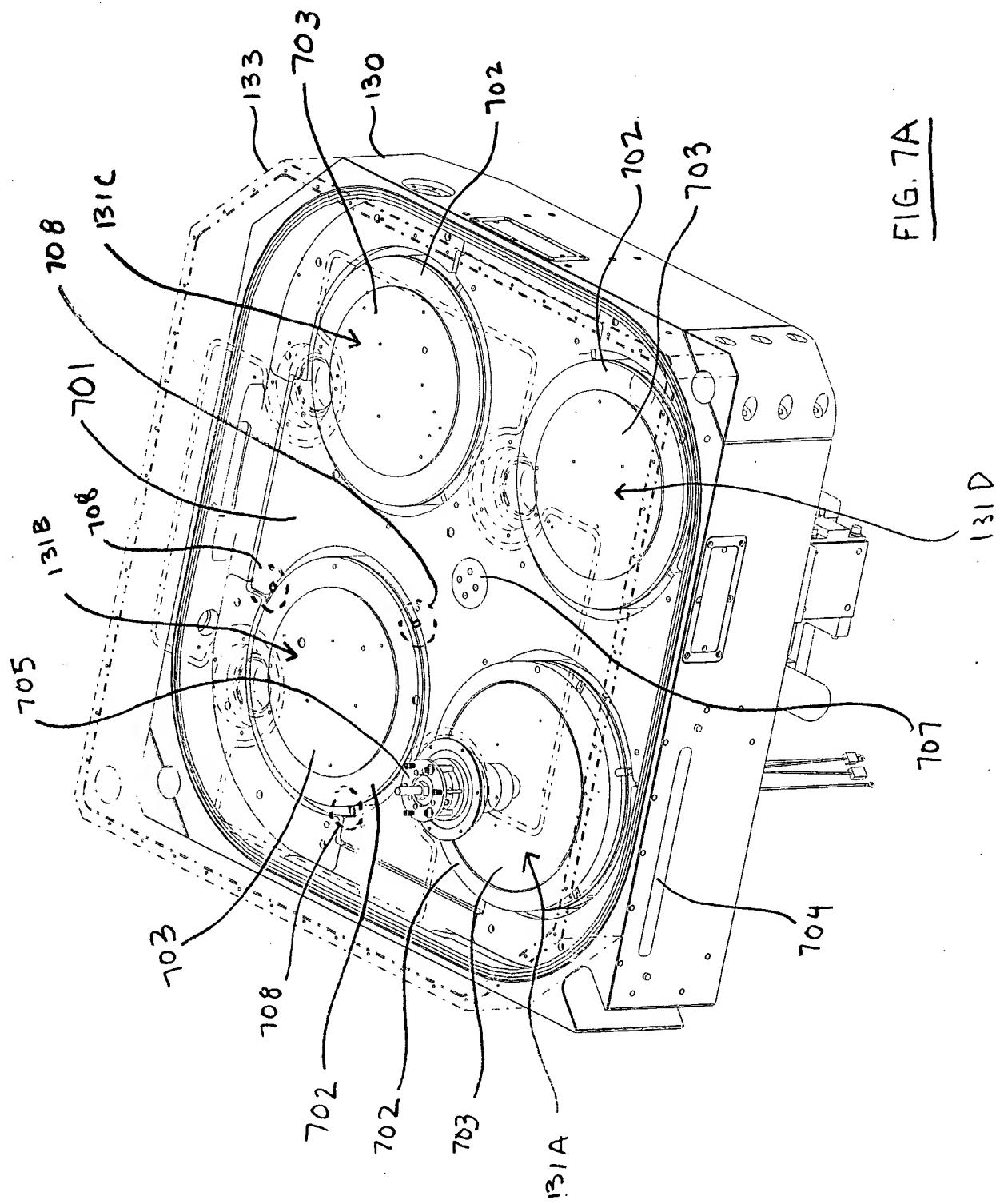
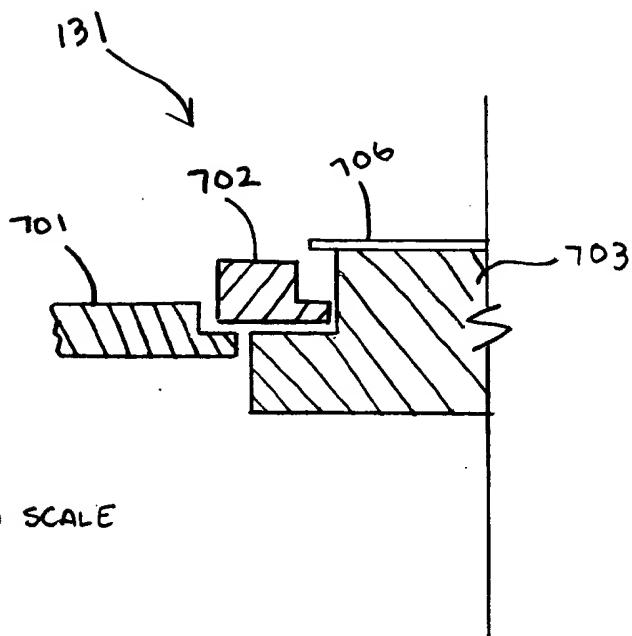


FIG. 6



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TITLE: HIGH THROUGHPUT ARCHITECTURE FOR
SEMICONDUCTOR PROCESSING



NOT TO SCALE

FIG. 7B

